IN THE SPECIFICATION

Please insert the following before line 5 on page 2:

CROSS-REFERENCE TO RELATED APPLICATION

This is a divisional of co-pending application Serial No. 10/210,932 filed August 2, 2002.

Please replace the paragraph beginning on page 6, line 2, with the following amended paragraph:

The present invention is generally directed to various methods of using ion implantation techniques to control various metal formation processes. In one illustrative embodiment, the method comprises forming a metal seed layer above a patterned layer of insulating material, the patterned layer of insulating material defining a plurality of field areas, deactivating at least a portion of the metal seed layer in areas where the metal seed layer is positioned above at least some of the field areas, and performing a deposition process to deposit a ~~meal~~ metal layer above the metal seed layer. In some embodiments, the metal seed layer may be comprised of copper, platinum, nickel, tantalum, tungsten, cobalt, silver or gold. In further embodiments, an ion implant process may be performed to deactivate portions of the metal seed layer. The implanted ions may be comprised of nitrogen, carbon, silicon or hydrogen.

Please replace the paragraph beginning on page 13, line 12, with the following amended paragraph:

After the ion implant process is completed, a bulk metal layer 70, *e.g.*, a bulk copper layer 70, may be formed in the features 32, 35 in the patterned layer of insulating material 33 by performing known electroplating or electroless processes. The bulk metal may also be comprised of copper, platinum, nickel, tantalum, tungsten, cobalt, silver or gold. Note that, due to the ion implant regions 52 in the metal seed layer 38, little or no metal is formed above the field regions 31 of the device. Although the wider feature 35 will still take longer to fill than the smaller feature 32, less excess metal will be generated above the features 32 and the field areas 31. As a result, subsequent chemical mechanical polishing processes may be performed in a more efficient manner. Figure ~~2G~~ 2H is a depiction of the device after a CMP process has been performed to remove the excess metal and the barrier metal layer 36 from above the surface of the patterned insulating layer 33. That is, CMP operations are performed until such time as the upper surface 71 of the conductive copper structures 73 is approximately planar with the upper surface 37 of the patterned layer of insulating material 33. This process may be repeated layer after layer as the wiring pattern for the device is formed in multiple levels of insulating material. Moreover, the present invention may be employed with a variety of different techniques for forming such conductive interconnections, *e.g.*, single damascene, dual damascene, etc.